Dr. Mahalingam College of Engineering and Technology

(An Autonomous Institution)

Pollachi - 642003

Curriculum and Syllabus for

M.E. APPLIED ELECTRONICS

Revision 0

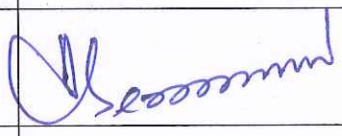
REGULATIONS 2014

DR MAHALINGAM MCET

COLLEGE OF ENGINEERING AND TECHNOLOGY

Enlightening Technical Minds

Programme : M.E. – Applied Electronics
Curriculum and Syllabus – Revision 0
Approved by Academic Council

Action	Responsibility	Signature of Authorized Signatory
Designed and Developed by	BoS Applied Electronics	
Compiled by	Office of COE	
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Department of Electrical and Electronics Engineering

Curriculum for M.E. Applied Electronics

Regulations 2014 - Revision 0

Semester I

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
140AE0101	Applied Mathematics	3	1	0	4	100
140AE0102	Advanced Digital Signal Processing	3	1	0	4	100
140AE0103	Advanced Digital System Design	3	0	0	3	100
140AE0104	VLSI Design Techniques	3	0	0	3	100
140AE0105	Industrial Electronics	3	0	0	3	100
xxx	Elective– I	3	0	0	3	100
PRACTICAL						
140AE0107	Applied Electronics Design Laboratory I	0	0	3	2	100
Total		**18**	**2**	**3**	**22**	**700**

SEMESTER II

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
140AE0201	Analysis and Design of Analog Integrated Circuits	3	1	0	4	100
140AE0202	Embedded Systems	3	0	0	3	100
140AE0203	CAD of VLSI Circuits	3	0	0	3	100
140AE0204	Digital Control Engineering	3	0	0	3	100
xxx	Elective– II	3	0	0	3	100
xxx	Elective –III	3	0	0	3	100
PRACTICAL						
140AE0207	Applied Electronics Design Laboratory II	0	0	3	2	100
Total		**18**	**1**	**3**	**21**	**700**

BoS Chairman

SEMESTER III

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
THEORY						
xxx	Elective –IV	3	0	0	3	100
xxx	Elective –V	3	0	0	3	100
xxx	Elective– VI	3	0	0	3	100
PRACTICAL						
140AE0307	Project Work Phase I	0	0	12	6	200
TOTAL		**9**	**0**	**12**	**15**	**500**

SEMESTER IV

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
PRACTICAL						
140AE0407	Project Work Phase II	0	0	24	12	400
TOTAL		**0**	**0**	**24**	**12**	**400**

Total Credits: 70

LIST OF ELECTIVES

Course Code	Course Title	Hours/Week			Credits	Marks
		L	T	P		
140AE9111	Project Management	3	0	0	3	100
140AE9112	Advanced Microprocessors	3	0	0	3	100
140AE9113	Programming with VHDL	3	0	0	3	100
140AE9114	Digital Image Processing	3	0	0	3	100
140AE9115	Soft Computing Techniques	3	0	0	3	100
140AE9116	Power Quality Engineering	3	0	0	3	100
140AE9117	ASIC Design	3	0	0	3	100
140AE9118	Data Communication Networks	3	0	0	3	100
140AE9119	Virtual Instrumentation Systems	3	0	0	3	100
140AE9120	Nano computing	3	0	0	3	100
140AE9121	VLSI Signal Processing	3	0	0	3	100
140AE9122	High Performance Switching Architectures	3	0	0	3	100
140AE9123	MEMS System Design Concepts	3	0	0	3	100
140AE9124	Wavelet Transforms and its Applications	3	0	0	3	100
140AE9125	Low Power VLSI Design	3	0	0	3	100
140AE9126	Internetworking and multimedia	3	0	0	3	100
140AE9127	Algorithm Analysis and Design	3	0	0	3	100
140AE9128	Research Methodology	3	0	0	3	100
140AE9129	Speech and Audio Signal Processing	3	0	0	3	100

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SEMESTER I

140AE0101 **APPLIED MATHEMATICS** **3 1 0 4**

AIM:

To enhance the mathematical knowledge of the students and develop the skills in determining the solutions of problems related to their field.

OBJECTIVES:

- To introduce the fundamental ideas of linear algebra.
- To introduce the concepts of eigen values and eigen vectors.
- To introduce the concepts of linear programming and non linear programming.

UNIT I LINEAR EQUATIONS AND VECTOR SPACES **9+3**

System of linear equations – Row reduction and Echelon forms – Application of linear systems –Vector spaces and subspaces and linear transformations – Linearly independent sets; Bases Dimension of a vector space – Coordinate systems.

UNIT II MATRIX ALGEBRA **9+3**

Inverse of a matrix – Characteristics of invertible matrices – Partitioned matrices – Matrix factorizations – Dimension and rank – Eigen values & Eigen vectors – Characteristic equation – Diagonalization of symmetric matrices – Quadratic forms – Applications to differential equations – Iterative estimates for Eigen values – Applications to image processing.

UNIT III ORTHOGONALITY AND LEAST SQUARES **9+3**

Inner product, length and Orthogonality – Orthogonal sets – Orthogonal projections – Gram – Schmidt process – Least square problems – Inner product spaces – Applications of inner product spaces.

UNIT IV LINEAR PROGRAMMING **9+3**

Simplex algorithm – Two–phase and Big–M method – Duality theory – Dual simplex method – Transportation and Assignment problems.

UNIT V NON – LINEAR PROGRAMMING **9+3**

Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Saddle point problem – Graphical method of non–linear programming problem involving only two variables – Kuhn–tucker conditions with non–negative constraints – Wolfe's modified simplex method.

L: 45, T: 15, Total: 60

REFERENCES:

1. David C Lay, "Linear Algebra and its Applications", Pearson Education Asia, New Delhi, 2003.
2. Gilbert Strang, "Linear Algebra and its Applications", Brooks/Cole Ltd., New Delhi, 3rd Edition, 2003.
3. Seymour Lipschutz and Marc Lipson, "Schaum's Outline of Linear Algebra", McGraw Hill Trade,New Delhi, 3rd Edition, 2000.
4. Howard A Anton "Elementary Linear Algebra", John Wiley & Sons, Singapore, 8th Edition 2000.
5. Gupta. P.K, Hira. D.S, "Operations Research", S.Chand &Co ., 1999.

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BoS Chairman

140AE0102 **ADVANCED DIGITAL SIGNAL PROCESSING** **3 1 0 4**
(Common to AE and CM Programmes)

AIM:
To provide students with a solid understanding of a number of important and related advanced topics in digital signal processing such as filters, power spectrum estimation, signal modeling and adaptive filtering.

OBJECTIVES:
- Understand the concepts of discrete random processes.
- Compute the spectral estimation by non parametric methods.
- Apply various estimators and predictor to filters.
- Compare FIR and IIR adaptive filters.
- Know the concepts of multirate DSP.
- Application of sub–band coding.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING **9+3**
Discrete Random Processes – Ensemble Averages, Stationary processes, Bias and Estimation, Auto covariance, Autocorrelation, Parseval's theorem, Wiener – Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION **9+3**
Estimation of spectra from finite duration signals, Nonparametric methods – Periodogram, Modified periodogram, Bartlett, Welch and Blackman –Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson–Durbin algorithm.

UNIT III LINEAR ESTIMATION AND PREDICTION **9+3**
Linear prediction – Forward and Backward prediction, Solution of Prony's normal equations, Least mean squared error criterion, Wiener filter for filtering and prediction, FIR and IIR Wiener filters, Discrete Kalman filter.

UNIT IV ADAPTIVE FILTERS **9+3**
FIR adaptive filters – adaptive filter based on steepest descent method – Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive filters, Exponentially Weighted RLS, Sliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING **9+3**
Mathematical description of change of sampling rate – Interpolation and Decimation, Decimation by an integer factor, Interpolation by an integer factor, sampling rate conversion by a rational factor, Polyphase filter structures, Multistage implementation of Multirate system, Application to subband coding – Wavelet transform.

L: 45, T: 15, Total: 60

REFERENCES:

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2007.
3. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education Inc., 2nd Edition, 2004 (For Wavelet Transform Topic).

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BoS Chairman

140AE0103 **ADVANCED DIGITAL SYSTEM DESIGN** **3 0 0 3**

AIM:

To enhance the knowledge to the students about advanced digital circuit design and its fault identification and the VHDL language for its design.

OBJECTIVES:

- To design and analyze the synchronous and asynchronous sequential circuits.
- To introduce the concepts of fault diagnosis and testability algorithms in digital circuit.
- To implement the logic circuit design in programmable devices.
- To give an exposure to the VHDL language.

UNIT I SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of clocked synchronous sequential circuits and modeling – State diagram, state table, state table assignment and reduction – Design of synchronous sequential circuits – design of iterative circuits – ASM chart and realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of asynchronous sequential circuit – flow table reduction – races – state assignment –transition table and problems in transition table – design of asynchronous sequential circuit – Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS **9**

Fault table method–path sensitization method – Boolean difference method – D algorithm –Tolerance techniques – The compact algorithm – Fault in PLA – Test generation – DFT schemes – Built in self test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES **9**

Programming Techniques – Re–Programmable Devices Architecture – Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT V NEW GENERATION PROGRAMMABLE LOGIC DEVICES **9**

Foldback Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 – Xilinx 3000.

L: 45, T: 0, Total: 45

REFERENCES:

1. Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Deisgn", Tata McGraw Hill, 2002.
3. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education, 2004.
4. Parag K Lala, "Digital System design using PLD", BS Publications, 2003.
5. John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001.
6. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001.
7. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

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BoS Chairman

140AE0104 **VLSI DESIGN TECHNIQUES** **3 0 0 3**

AIM:

To enhance the knowledge on VLSI design techniques and Verilog HDL to the students.

OBJECTIVES:

- To introduce the concepts of VLSI technology and circuit design processes.
- To introduce the concepts of VLSI fabrication technology.
- To provide an exposure to the students on design of various VLSI based systems.
- To give an exposure to the students on Verilog HDL.

UNIT I OVERVIEW OF VLSI DESIGN TECHNOLOGY **9**

The VLSI design process – Architectural design – Logical design – physical design – Layout styles – Full custom – Semi custom approaches – Basic electrical properties of MOS and CMOS circuits: Ids versus Vds relationships – Transconductance – pass transistor – nMOS inverter – Determination of pull up to pull down ratio for an nMOS inverter – CMOS inverter – MOS transistor circuit model.

UNIT II VLSI FABRICATION TECHNOLOGY **9**

Overview of wafer fabrication – wafer processing – oxidation – patterning – Diffusion – Ion implantation – Deposition – Silicon gate nMOS process – nwell CMOS process – pwell CMOS process – Twintub process – Silicon on insulator.

UNIT III MOS AND CMOS CIRCUIT DESIGN PROCESS **9**

MOS layers – Stick diagrams – nMOs design style – CMOS design style – Design rules and layout – Lambda based design rules – Contact cuts – Double metal MOS process rules – CMOS lambda based design rules – Sheet resistance – Inverter delay – Driving large capacitive loads – Wiring capacitance.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN **9**

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High–speed adders, Multipliers – Physical design – Delay modelling , cross talk, floor planning, power distribution – Clock distribution – Basics of CMOS testing.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE **9**

Overview of digital design with Verilog HDL – hierarchical modeling concepts – modules and port definitions – gate level modeling – data flow modeling – behavioral modeling – task & functions – Test Bench.

L: 45, T: 0, Total: 45

REFERENCES:

1. Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley and Sons, Inc., 2002.
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill Int. Ed., 1990.
5. Bhasker. J., B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
7. Wayne Wolf, "Modern VLSI Design System on chip", Pearson Education,2002.

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BoS Chairman

140AE0105 **INDUSTRIAL ELECTRONICS** **3 0 0 3**

AIM:

To expose the students to the concepts of various power semiconductor devices and its role in power converter circuits.

OBJECTIVES:

- To impart knowledge on constructional details, principle of operation, characteristics and firing circuit of thyristors, Power MOSFET and IGBT.
- To provide knowledge on principle of operation of power converters used in wind and solar systems.
- To impart knowledge on principle of operation of resonant converters.
- To give exposure on practical applications of converters.

UNIT I POWER SEMICONDUCTOR DEVICES **9**

THYRISTORS: Physics of device operation – Electrical rating – Types of thyristors: Asymmetrical thyristor, Reverse conducting thyristors, light fired thyristors – Turn-on and off mechanisms – Series and parallel operation of thyristors.

POWER MOSFETS: Types – Comparison with BJT – Structure – Principle of operation – Switching characteristics.

IGBTS: Comparison with power BJT and MOSFET – Structure – Principle of working – Switching characteristics – HV IGBT structure – Principle of working – Comparison with GTO.

UNIT II FIRING AND PROTECTION CIRCUITS **9**

Necessity of isolation, pulse transformer, opto coupler – Gate drive circuit: SCR, MOSFET, IGBTs and base drive circuit for power BJT, digital firing schemes – Over voltage, over current and gate protections – Design of snubber circuit.

UNIT III POWER CONVERTERS IN WIND AND SOLAR SYSTEMS **9**

Solar: Block diagram of solar photo voltaic system – Principle of operation: line commutated converters (inversion–mode) – Boost and buck–boost converters – selection of inverter, battery sizing, array sizing.

Wind: Principle of operation: Three phase AC voltage controllers, Uncontrolled and Controlled rectifiers, PWM Inverters, Grid Interactive Inverters, Matrix converters.

UNIT IV RESONANT CONVERTERS **9**

Zero voltage and Zero current switching – Classification of resonant converters –Basic resonant circuit concepts – Load resonant converters – Resonant switch converters – Zero voltage switching, clamped voltage topologies – Resonant DC link Inverters and Zero voltage switching – High frequency link integral half cycle converters.

UNIT V APPLICATIONS **9**

Linear regulators: Switching regulators – Concept of switched mode power supply – Uninterruptible power supply: Different configurations and applications– Speed control of ac and dc drives – Static Circuit Breakers – Solid state relays.

L: 45, T: 0, Total: 45

REFERENCES:

1. Muhammad H. Rashid, "Power Electronics – Circuits, Device and Applications", Pearson, Prentice – Hall of India Private Ltd., New Delhi, 3rd Edition, 2011.
2. Ned Mohan et.al. "Power Electronics – Converters, Applications and Design", John Wiley and Sons (Asia) Private Ltd., 2006.
3. Dubey, G.K., Doradia, S.R., Joshi, A. and Sinha, R.M., "Thyristorised Power Controllers", New age international publishers, 2003.
4. Joseph Vithayathil, "Power Electronics – Principles and Applications", Tata McGraw Hill, 2010.
5. Dr. Bimbhra. P.S., "Power Electronics ", Khanna Publishers, 4th edition, 2008.
6. Mukund R Patel, "Wind and Solar Power Systems", CRC Press, 2004.

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BoS Chairman

140AE0107 APPLIED ELECTRONICS DESIGN LABORATORY I 0 0 3 2

AIM:

To give the experience and practice in using SPICE, MATLAB and HDL to the students.

OBJECTIVES:

- To provide hands-on experience on design and simulation of electronic circuits using PSPICE and MATLAB.
- To provide hands-on experience in FPGA implementations of 4-bit ALU and Real Time Clock.

LIST OF EXPERIMENTS:

1. Design of NMOS/PMOS Logic gates using SPICE.
2. Design of Dynamic latches using SPICE.
3. Design and Simulation of Operational Amplifier using SPICE.
4. Design and Simulation of Analog Multiplier using SPICE.
5. Design of Switched Capacitor filters using SPICE.
6. Design and Simulation of Digital circuits using HDL.
7. FPGA Implementation of 4 Bit ALU.
8. FPGA Implementation of Real Time Clock.
9. Simulation of adaptive and non adaptive digital control system using MATLAB.
10. Design of PLL using MATLAB.

Total: 45

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BoS Chairman

SEMESTER II

140AE0201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 1 0 4

AIM:

To enhance the knowledge to the students about Bipolar and MOS transistors and their design and analysis for circuit configuration.

OBJECTIVES:

- To understand the models for integrated circuit active devices.
- To study the circuit configuration for linear IC.
- To understand the concepts of operational amplifiers.
- To give an exposure analog multiplier and PLL.
- To develop the knowledge of analog design using MOS technology.

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 12+3

Depletion region of a PN junction – large signal behavior of bipolar transistors – small signal model of bipolar transistor– large signal behavior of MOSFET – small signal model of the MOS transistors – short channel effects in MOS transistors – weak inversion in MOS transistors – substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9+3

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references – Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 8+3

Analysis of operational amplifiers circuit – slew rate model and high frequency analysis – Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL 10+3

Analysis of four quadrant and variable transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise– Noise models of Integrated – circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 6+3

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic – Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

L: 45, T: 15, Total 60

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", 4th Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000.
3. Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuitd", 3rd Edition, McGraw Hill, 2001.
4. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modeling and Technology", Prentice Hall of India pvt. ltd, 2004.
5. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley and sons,Inc.,2003.
6. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition–Oxford University Press, 2003.

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BoS Chairman

140AE0202 **EMBEDDED SYSTEMS** **3 0 0 3**

AIM:

To make students to understand the blocks of embedded system and programming.

OBJECTIVES:

- To deal with product design and characteristics of embedded computer application.
- To know about different controllers and parallel protocols.
- To understand the concept of programming in embedded systems, Routines, Queues, Pointers, etc.,
- To have knowledge about design cycle and tools for development of embedded system.
- To study about real time applications of embedded systems.

UNIT I INTRODUCTION **6**

Building Blocks of an embedded system – Overview of dedicated and automated system and their requirements Characteristics of embedded computer applications – The product design cycle – Design challenges in embedded system Design – Design Technology.

UNIT II PERIPHERALS, MEOMORY AND I/O INTERFACING **12**

Timers, Counter and Watch dog Timer – UART – Pulse Width Modulator – LCD Controllers – Key Pad Controllers – Stepper Motor Controllers – Analog to Digital Converters, Memory Types – ROM –EPROM – EEPROM – Flash Memory – RAM – SRAM – Cache Memory – Memory Management Unit – Interrupts – DMA – Serial Protocols – I^2C – CAN – USB – Parallel Protocols – PCI Bus – ARM Bus.

UNIT III EMBEDDED PROGRAMMING **9**

Programming in Assembly Language (ALP) Vs High level language – C program elements, Macros and Functions – Use of pointers – NULL pointers – use of function calls – multiple function calls in a cyclic order in the main function pointers – Function queues and interrupt service Routines queues pointers – Concepts of Embedded programming in C++ – Object oriented programming – Embedded programming in C++, C program compilers – Cross compiler – optimization of memory codes.

UNIT IV EMBEDDED SYSTEM CO–DESIGN **9**

Embedded System project management – Embedded system design and Co–Design Issues in System Development process – Design cycle in the development phase for an embedded system – Uses of Target system or its emulator and In–Circuit Emulator – Use of software Tools for Development of an embedded system – Use of scopes and logic analyzers for system hardware tests – Issues in Embedded System Design.

UNIT V REAL–TIME OPERATING SYSTEMS **9**

Operating system services – I/O subsystems – Network operating systems – Interrupt Routines in RTOS Environment – RTOS Task scheduling models, Interrupt – Performance Metric in Scheduling Models – IEEE standard POSIX functions for standardization of RTOS and inter – task communication functions – List of Basic functions in a Preemptive scheduler – Fifteen point strategy for synchronization between processors, ISRs, OS Functions and Tasks – OS security issues – Mobile OS.

L: 45, T: 0, Total 45

REFERENCES:

1. Frank Vahid and Tony Givargis, "Embedded System Design: A unified Hardware/ Software Introduction", John Wiley and sons, 2002.
2. Arnold Berger, "Embedded System Design: An Introduction to Processes, Tools & Techniques", CMP Books, Dec 2001.
3. Steve Heath, "Embedded Systems Design", Butterworth – Heinemann, Nov 1997.
4. Wayne Wolf, "Computers as Components: Principles of Embedded Computer Systems Design", Morgan– Kaufmann, Sep 2000.
5. Valvino J W, "Embedded micro computer system: Real time Interfacing", Brooks/ cole, 2000.
6. RajKamal, "Embedded System–Architecture, Programming, Design", Tata McGraw Hill, New Delhi, 2003.

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BoS Chairman

140AE0203 **CAD OF VLSI CIRCUITS** **3 0 0 3**

AIM:

To provide a broad exposure to the algorithms and data structures to generate the layout of modern VLSI design tools.

OBJECTIVES:

- To understand algorithmic graph theory.
- To solve combinatorial optimization problems by various algorithms.
- To know the Algorithms for Placement and Partitioning.
- To study the concepts of floor planning.
- To model and simulate VLSI circuits.
- To know principles of Binary–decision Diagrams.

UNIT I DESIGN METHODOLOGIES **9**

Introduction to VLSI Design methodologies – Review of VLSI Design automation tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – general purpose methods for combinatorial optimization.

UNIT II LAYOUT DESIGN – I **8**

Layout Compaction – Design rules – problem formulation – algorithms for constraint graph compaction – placement and partitioning – Circuit representation – Placement algorithms – partitioning.

UNIT III LAYOUT DESIGN – II **9**

Floor planning concepts – shape functions and floor plan sizing – Types of local routing problems – Area routing – channel routing – global routing – algorithms for global routing.

UNIT IV SIMULATION AND SYNTHESIS **10**

Simulation – Gate–level modeling and simulation – Switch–level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS **9**

High level Synthesis – Hardware models – Internal representation – Allocation – assignment and scheduling – Simple scheduling algorithm – Assignment problem – High level transformations.

L: 45, T: 0, Total 45

REFERENCES:

1. Gerez. S.H., "Algorithms for VLSI Design Automation", John Wiley and Sons,2002.
2. Sherwani. N.A., "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
3. Drechsler, R., "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, Boston, 1998.
4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, Boston, 1989.

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BoS Chairman

140AE0204 **DIGITAL CONTROL ENGINEERING** **3 0 0 3**

AIM:

To enhance knowledge in the advanced concepts of control theory and digital design of control engineering.

OBJECTIVES:

- To understand the basic time and frequency response analysis and discrete time signals.
- To provide adequate knowledge on models of digital control devices and systems.
- To give basic knowledge in obtaining the state variables.
- To understand the concept of stability of control system and methods of stability analysis.
- To study the design of digital control systems.

UNIT I INTRODUCTION **10**

Overview of frequency and time response analysis and specifications of control systems – Digital control systems – basic concepts of sampled data control systems – principle of sampling, quantization and coding – Reconstruction of signals – Sample and Hold circuits – Practical aspects of choice of sampling rate – Basic discrete time signals – Time domain models for discrete time systems.

UNIT II MODELS OF DIGITAL CONTROL DEVICES AND SYSTEMS **9**

Z domain description of sampled continuous time plants – models of A/D and D/A converters – Z Domain description of systems with dead time – Implementation of digital controllers – Digital PID controllers – Position, velocity algorithms – Tuning – Zeigler – Nichols tuning method.

UNIT III STATE VARIABLE ANALYSIS **9**

State space representation of discrete time systems – Solution of discrete time state space equation – State transition matrix – Decomposition techniques – Controllability and Observability – Multi variable discrete systems.

UNIT IV STABILITY ANALYSIS **8**

Mapping between S plane and Z plane– Jury's stability test – Bilinear transformation and extended Routh array– Root Locus Method –Liapunov Stability Analysis of discrete time systems.

UNIT V DESIGN OF DIGITAL CONTROL SYSTEM **9**

Z plane specifications of control system design – Digital compensator design – Frequency response method – State feed back – Pole placement design – State Observers – Digital filter properties – Frequency response – Kalman's filter.

L:45, T: 0, Total 45

REFERENCES:

1. Gopal M. "Digital Control and State Variable methods", Tata Mc Graw Hill Publishing Company Ltd., New Delhi, India, 2003.
2. Kuo B.C. " Digital Control Systems", Oxford University Press, Inc., 2003
3. Ogata K. "Discrete Time Control Systems", Prentice Hall International, New Gercy, USA, 2002.
4. Houpis C.H. and Lamont C.B., "Digital Control Systems", Tata Mc Graw Hill,1999.

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BoS Chairman

140AE0207 **APPLIED ELECTRONICS DESIGN LABORATORY II** **0 0 3 2**

AIM:

To enhance the students knowledge in Microcontrollers and DSP Processors and their applications.

OBJECTIVES:

- To provide hands-on experience in developing the programs using embedded controllers and DSP processors.
- To understand the concepts of interfacing using embedded processors.

LIST OF EXPERIMENTS:

1. LED and Key Matrix interface using Embedded Microcontroller.
2. LCD Interface using Embedded Microcontroller.
3. Rolling Display in LCD /LED using Embedded Microcontroller.
4. EEPROM Interface using Embedded Microcontroller.
5. RTC using Embedded Microcontroller.
6. ADC and DAC Interface using Embedded Microcontroller.
7. Stepper Motor Interface using Embedded Microcontroller.
8. Matrix Multiplication using DSP Processor.
9. Design and Implementation of Convolution Algorithm using DSP Processor.
10. Echo Cancellation using DSP Processor.

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BoS Chairman