Question Bank

VLSI-DESIGN

DEPARTMENT OF

ELECTRONICS AND INSTRUMENTATION

ENGINEERING

UNIT -1 CMOS TECHNOLOGY

PART-A

1.List the advantages of SOI CMOS process

- Denser transistor structures are possible.

- Lower substrate capacitances

- No field inversion problem

- No latch up

- No body effect problem

- Enhanced radiation tolerance

2. Distinguish electrically alterable & non-electrically alterable ROM

In electrically alterable ROM the cell can be turned ON or OFF by controlling the voltages applied to the control gate, source and drain voltages. In non-electrically alterable ROM versions, the process can only be reversed by illuminating the gate with UV light.

3. How do you prevent latch up problem?

Latch up problem can be reduced by reducing the gain of parasitic transistors and resistors. It can be prevented in 2 ways

- Latch up resistant CMOS program

- Layout technique

    The various lay out techniques are
            Internal latch up prevention technique
            I/O latch up prevention technique.

4.List the basic process for IC fabrication

    _ Silicon wafer Preparation
    _ Epitaxial Growth
    _ Oxidation
    _ Photolithography
    _ Diffusion
    _ Ion Implantation
    _ Isolation technique
    _ Metallization
    _ Assembly processing & Packaging

5.What are the various Silicon wafer Preparation?

  _ Crystal growth & doping
  _ Ingot trimming & grinding
  _ Ingot slicing
  _ Wafer polishing & etching
  _ Wafer cleaning.

6.Different types of oxidation?

Dry & Wet Oxidation

7.What are the advantages of CMOS process?

- Low power Dissipation
- High Packing density
- Bi directional capability
- Low Input Impedance
- Low delay Sensitivity to load.

8.What is pull down device?

  A device connected so as to pull the output voltage to the lower supply voltage usualy 0V is called pull down device.

9.What is pull up device?

  A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

10.. Why NMOS technology is preferred more than PMOS technology?

  N- channel transistors has greater switching speed when compared tp PMOS transistors.

11. What are the different operating regions foe an MOS transistor?
  _ Cutoff region

  _ Non- Saturated Region
  _ Saturated Region

12.What is Channel-length modulation?

  The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V_{DS}, increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

13. What is Latch – up?

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DD} and V_{SS} with disastrous results. Careful
control during fabrication is necessary to avoid this problem.

14. What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

15. What are the uses of Stick diagram?

_ It can be drawn much easier and faster than a complex layout.
_ These are especially important tools for layout built from large cells.

16. Give the various color coding used in stick diagram?

_ Green – n-diffusion
_ Red- polysilicon
_ Blue –metal
_ Yellow- implant

_ Black-contact areas.

18. Define Threshold voltage in CMOS?

The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

19. What is Body effect?

The threshold volatge V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

20. What are the various cmos technologies?

Various cmos technologies are,

I) n- well process or n -tub process
ii) p well process or p-tub process
iii) Twin tub process
iv) Silicon on Insulator (SOI) process

21. What is channel-stop implantation?

In n -well fabrication, n-well is protected with resist material. Because it should not be affected by boron implantation. Then boron is implanted except n-well. It is done using photo resist mask. This type of implantation is known as channel-stop implantation.

22.What is LOCOS?

LOCOS mean Local Oxidation of Silicon. This is one type of oxide construction.
23.What is SWAMI?

SWAMI means Side Wall Masked Isolation. It is used to reduce bird's beak effect.

24.What is LDD?

LDD means Lightly Doped Drain structures. It is used for implantation of n-in n-well process. T

25.What is twin tub process? Why it is so called?

Twin tub process is one of cmos technology. There are two wells available in this process. The other name of well is tub. so because of these two tubs, this process is known as twin tub process.

26.What are the special features of twin tub process?

In twin tub process, threshold voltages, body effect of n and p devices are independently optimized.

27.What are the advantages of twin tub process?

Advantages of twin tub process are
1) Separate optimized wells are available.
2) Balanced performance is obtained for n and p transistors.

28.What is SOI? What is the material used as insulator?

SOI means Silicon –On-Insulator. In this process, sapphire or sio2 is used as insulator.

29.What are the various etching processes used in SOI process?

Various etching process used in SOI are,
1) Isotropic etching process
2) Anisotropic etching process
3) Preferential etching process

30.What are the advantages and disadvantages of SOI process?

Advantages of SOI process

There is no well formation in this process
There is no field –Inversion problem.

There is no body effect problem.
Disadvantages of SOI process

It is very difficult to protect inputs in this process.

Device gain is low.
The coupling capacitance between wires always exists.

31.What is meant by interconnect? What are the types of interconnect?

Interconnect means connection between various components in an
IC Types of Interconnect
Metal Interconnect

Polysilicon Inter connect.
Local Inter Connect.

32.What is silicide?

The combination of Silicon and tantalum is known as Silicide. It is used as gate materials
in polysilicon interconnect.

33.What are the two types of Layout design rules?

Lambda (λ) design rules and micron rules are major types of layout design rules.

PART-B

1. Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage
at different region in the transfer characteristics.

2. Explain with neat diagrams the various CMOS fabrication technology

3. Explain the latch up prevention techniques.

4. Explain the operation of PMOS Enhancement transistor
5. Explain the silicon semiconductor fabrication process.
6. Explain various CAD tool sets.

UNIT – 2 CIRCUIT CHARACTERIZATION AND SIMULATION

PART-A
1.What is the fundamental goal in Device modeling?

To obtain the functional relationship among the terminal electrical variables of the
device that is to be modeled.
2.Define Short Channel devices?

Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.

3.What is pull down device?
A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

4.What is pull up device?
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5. Why NMOS technology is preferred more than PMOS technology? N- channel transistors has greater switching speed when compared tp PMOS transistors.

6. What are the different operating regions foe an MOS transistor?
_ Cutoff region

_ Non- Saturated Region
_ Saturated Region

7. What are the different MOS layers?
_ n-diffusion

_ p-diffusion
_ Polysilicon
_ Metal

8.What is Stick Diagram?

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_ These are especially important tools for layout built from large cells.

10.Give the various color coding used in stick diagram?
_ Green – n-diffusion

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_ Blue –metal
_ Yellow- implant

PART-B

1. Explain the latch up prevention techniques.
2. Explain the operation of PMOS Enhancement transistor
3. Explain the threshold voltage equation

4. Explain the silicon semiconductor fabrication process.

5. Explain the operation of NMOS Enhancement transistor.

6. Explain the Transmission gate and the tristate inverter briefly.
7. Explain about the various non ideal conditions in MOS device model.
8. Explain the design hierarchies.

UNIT 3 COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN

PART -A

1. **Which MOS can pass logic1 and logic 0 stongly?**

p-mos can pass strong logic 1

n-mos can pass strong logic 0.

2. What is meant by a transmission gate?

      A transmission gate consists of an n-channel transistor and p-channel transistor with separate gates and common source and drain.

3.Write the design style classification?

The IC design style can be classified as

(1) Full custom Design ASICs

(2) Semi custom Design ASICs
    (a) Standard Cell Design
    (b) Gate Array Design
        (i) Channeled Gate Array
        (ii) Channel less Gate Array
(3) Programmable ASICs
    (a) PLDs
    (b) FPGA

6.What are the two types of ASICs ?

      Types of ASICs are

      Full custom ASICs
      Semi custom ASICs

7.What are the types of programmable devices?

      Types of programmable devices are

            (1) Programmable Logic Structure

            (2) Programmable Interconnect.

(3) Reprogrammable Gate Array.

8.What are the different types of programming structure available in PAL?

Programming Techniques of PAL are

(1) Fusible links programming

(2) UV-Erasable EPROM programming
(3) EEPROM programming

9.Why CMOS technology is most useful for analog functions?

The first reason is that CMOS is now by far the most widely available IC technology. Most CMOS Asics and CMOS standard products are now being manufactured than bipolar ICs. The second reason is that increased levels of integration require mixing analog and digital functions on the same IC: this has forced designers to find ways to use CMOS technology to implement analog functions.

10.What are the features of standard celled ASICs?

All mask layers are customized- transistors and interconnect.

Custom blocks can be embedded.
Manufacturing lead time is about eight weeks.

11.What is the difference between channeled gate array and channel less gate array?

The key difference between a channelless gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channelless gate array. Instead we route over the top of the gate –array devices. We can do this because we customize the contact defines the connections between metal1, the first layer of metal and the transistors.

12.What are the characteristics of FPGA?

* None of the mask layers are customized

* A method for programming the basic logic cells and the interconnect.
* The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).
* A matrix of programmable interconnect surrounds the basic logic cells.

* Design turn around is a few hours.

13.What is programmable logic array?

A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an

output an output. This layout allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

14. What is mean by Programmable logic plane?

The Programmable logic plane is programmable read -only memory (PROM) array that allows the signals present on the devices pins (or the logical components of those signals) to be routed to an output logic macro cell.

15. Describe the steps in ASIC design flow?

- Design entry. Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry.

- Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a net list

  – a description of the logic cells and their connections.

- System partitioning. Divide a large system into ASIC- sized pieces.

- Prelayout simulation. Check to see if the design functions correctly.

- Floor planning. Arrange the blocks of the net list on the chip.

- Placement. Decide the locations of cells in a block.

- Routing. Make the connections between cells and blocks.

- Extraction. Determine the resistance and capacitance of the interconnect.

- Post layout simulation. Check to see the design still works with the added loads of the interconnect.

16. Give the application of PLA

Design and testing of digital circuits

17. What is the full custom ASIC design?

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

18. What is the standard cell-based ASIC design?

A cell-based ASIC (CBIC) USES PREDESIGNED LOGIC CELLS KNOWN AS STANDARD CELLS. The standard cell areas also called fle4xible blocks in a

CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

20. Give the constituent of I/O cell in
      22V10. 2V10 I/O cell consists of

      1. a register
      2. an output 4:1 mux
      3. a tristate buffer
      4. a 2:1 input mux

      * 12 inputs

      * 10 I/Os
      * product time 9 10 12 14 16 14 12 10 8
      * 24 pins

21. What is a FPGA?

      A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used toimplement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

22. What are the different methods of programming of PALs?
      The programming of PALs is done in three main ways:
      Fusible links

      UV – erasable EPROM

      EEPROM (E $_2$PROM) – Electrically Erasable Programmable ROM

23.What is an antifuse?

      An antifuse is normally high resistance (>). On application of appropriateΩ100M programming voltages, the antifuse is changed permanently to a low-resistance structure (200-500Ω).

24. What are the different levels of design abstraction at physical design.
      Architectural or functional level

      Register Transfer-level (RTL)
      Logic level

      Circuit level

25.What are macros?

The logic cells in a gate-array library are often called macros.

26. What are Programmable Interconnects ?

In a PAL, the device is programmed by changing the characteristics of the switching element. An alternative would be to program the routing.

27. What are the types of gate arrays in ASIC?

1) Channeled gate arrays
2) Channel less gate arrays
3) Structured gate arrays

PART- B

1. Explain the concept of MOSFET as switches
2. Explain the ASIC design flow with a neat diagram
3. Explain the concept of Delay estimation, logical effort and sizing of MOSFET.

UNIT 4 CMOS TESTING

PART – A

1.What are the different types of CMOS testing
Functionality tests

Manufacturing tests

2. What is the aim of adhoc test techniques

The adhoc test techniques are aimed at reducing the combinational explosion of testing.

3. Distinguish functionality test and manufacturing test

Functionality tests seek to verify that a chip as a whole is functionally equivalent to some specification, whereas manufacturing tests are used to verify that every gate operates as expected.

4. List any two faults that occur during manufacturing

1. Stuck at fault

   (a) Stuck at 0 fault
   (b) Stuck at 1 fault

2. SC & OC faults

(a) Short circuit model fault
(b) Open circuit model fault

5.What is the need for testing?

IC fabrication is very complex process. SO, there may be any imperfection occur in any one of the stage. This imperfection may affect the result. So testing is necessary to find out which IC is good and which IC is bad.

6. Write notes on functionality tests?

Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.

7. Write notes on manufacturing tests?

Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.

8. Mention the defects that occur in a chip?

a) layer-to-layer shorts
b) discontinous wires
c) thin-oxide shorts to substrate or well

9. Give some circuit maladies to overcome the defects? i. nodes shorted to power or ground

ii. nodes shorted to each other
iii. inputs floating/outputs disconnected

10. What are the tests for I/O integrity?

i. I/O level test
ii. Speed test
iii. I_{DD} test

11. What is meant by fault models?

Fault model is a model for how faults occur and their impact on circuits.

12. Give some examples of fault models?

i. Stuck-At Faults
ii. Short-Circuit and Open-Circuit Faults

13. What is stuck – at fault?

With this model, a faulty gate input is modeled as a "stuck at zero" or "stuck at one". These faults most frequently occur due to thin-oxide shorts or metal-to-metal shorts.

14. What is meant by observability?

The observability of a particular internal circuit node is the degree to which one can observe that node at the outputs of an integrated circuit.

15. What is meant by controllability?

The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

16. What is known as percentage-fault coverage?

The total number of nodes that, when set to 1 or 0, do result in the detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage.

17. What is fault grading?

Fault grading consists of two steps. First, the node to be faulted is selected. A simulation is run with no faults inserted, and the results of this simulation are saved. Each node or line to be faulted is set to 0 and then 1 and the test vector set is applied. If and when a discrepancy is detected between the faulted circuit response and the good circuit response, the fault is said to be detected and the simulation is stopped.

18. Mention the ideas to increase the speed of fault simulation?

    a. parallel simulation
    b. concurrent simulation

19. What is fault sampling?

An approach to fault analysis is known as fault sampling. This is used in circuits where it is impossible to fault every node in the circuit. Nodes are randomly selected and faulted. The resulting fault detection rate may be statistically inferred from the number of faults that are detected in the fault set and the size of the set. The randomly selected faults are unbiased. It will determine whether the fault coverage exceeds a desired level.

20. What are the approaches in design for testability?

    a. ad hoc testing
    b. scan-based approaches
    c. self-test and built-in testing

21. Mention the common techniques involved in ad hoc testing?

        d. partitioning large sequential circuits
        e. adding test points
        f. adding multiplexers
        g. providing for easy state reset

22. What are the scan-based test techniques?

        a) Level sensitive scan design
        b) Serial scan
        c) Partial serial scan
        d) Parallel scan

23. What are the two tenets in LSSD? a.
        The circuit is level-sensitive.

        b.Each register may be converted to a serial shift register.

23. What are the self-test techniques? a.
        Signature analysis and BILBO
b. Memory self-test
        c. Iterative logic array testing

24. What is known as BILBO?

        Signature analysis can be merged with the scan technique to create a
structure known as BILBO- for Built In Logic Block Observation.

25. What is known as IDDQ testing?

        A popular method of testing for bridging faults is called IDDQ or
currentsupply monitoring. This relies on the fact that when a complementary CMOS
logic gate is not switching, it draws no DC current. When a bridging fault occurs,
for some combination of input conditions a measurable DC I_{DD} will flow.

26. What are the applications of chip level test techniques?

        a. Regular logic arrays
        b. Memories
        c. Random logic

27. What is boundary scan?

        The increasing complexity of boards and the movement to technologies
like multichip modules and surface-mount technologies resulted in system
designers agreeing on a unified scan-based methodology for testing chips at the
board. This is called boundary scan.

28. What is the test access port?

The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in a boundary-scan architecture. The port has four or five single bit connections, as follows:

TCK(The Test Clock Input)

TMS(The Test Mode Select)

TDI(The Test Data Input)

TDO(The Test Data Output)

It also has an optional signal

TRST*(The Test Reset Signal)

29. What are the contents of the test architecture?
The test architecture consists of:

The TAP interface pins A
set of test-data registers
An instruction register A
TAP controller

30. What is the TAP controller?

The TAP controller is a 16-state FSM that proceeds from state to state based on the TCK and TMS signals. It provides signals that control the test data registers, and the instruction register. These include serial-shift clocks and update clocks.

31. What is known as test data register?

The test-data registers are used to set the inputs of modules to be tested, and to collect the results of running tests.

32. What is known as boundary scan register?
The boundary scan register is a special case of a data register. It allows circuit-board interconnections to be tested, external components tested, and the state of chip digital I/Os to be sampled.

33. Mention the levels at which testing of a chip can be done?
a) At the wafer level
b) At the packaged-chip level
c) At the board level

d) At the system
level e) In the field

PART - B

1. Explain fault models.
A) Stuck-At Faults

B) Explain ATPG.
2. Briefly explain
a) Fault grading & fault simulation
b) Delay fault testing

c) Statistical fault analysis

3. Explain scan-based test techniques.

4. Explain Ad-Hoc testing and chip level test techniques.

5. Explain self-test techniques and IDDQ testing.

6. Explain system-level test techniques.

UNIT 5 SPECIFICATION USING VERILOG HDL

1. What is meant by continuous assignment statement in verilog HDL?

A continuous assignment assigns a value to a net. The syntax is assign_LHS target =
RHS _ expression;

Ex: assign Z = (A I B) ;

2. What is a task in verilog?

A task is like a procedure, it provides the ability to execute common pieces of code from
several different places in a description

3.Mention few data types in Verilog

Nets, registers, vectors, numbers and arrays

4.Mention the four key words used for looping in verilog

while, for, repeat, forever

5.Give the basic difference between tasks and functions.

Functions always return a single value. They cannot have output or in-out arguments. Tasks don't return a value, but can pass multiple values through output and inout arguments.

6.Specify the operator which have highest and lowest precedence.

Unary operator – highest precedence

Conditional operator – lowest precedence
7.what are bit wise operators in verilog?
Bit wise operators are,

| - binary or

~ - Unary negation
^ - Exclusive –or
~ ^ - Exclusive –nor &
- and
8.Give the examples for procedural statement.

Loop statement

Wait statement
Conditional statement
Case statement

9.In behavioral modeling specify the two most basic statements.

Initial and always statements

10.Blocking and non-blocking statements differ in executing the statements . How?

Blocking statements are executed in the order in which they are specified in a sequential block. "= "is the operator used to specify blocking assignments.

Non blocking statements allow scheduling of assignments without blocking execution of the statement that follow in a sequential block.
"<=" is the operator used to specify non blocking assignment.

11.Specify the three method of timing control.

Delay based timing control

Event based timing control

Level sensitive timing control

8. What are the various modeling used in Verilog?

    1. Gate-level modeling
    2. Data-flow modeling
    3. Switch-level modeling
    4. Behavioral modeling

9. What is the structural gate-level modeling?

Structural modeling describes a digital logic networks in terms of the components that make up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.

10. What is Switch-level modeling?

Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.

11. What are identifiers?

Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(_) and the dollar sign($). It must be a single group of characters.
Examples: A014, a ,b, in_o, s_out

12. What are the value sets in Verilog?

Verilog supports four levels for the values needed to describe hardware referred to as value sets.

13. Value levels Condition in hardware circuits

    0 Logic zero, false condition
    1 Logic one, true condition
    X Unknown logic value
    Z High impedance, floating state

14. Give the classifications of timing control?
    Methods of timing control:
    1. Delay-based timing control
    2. Event-based timing control
    3. Level-sensitive timing control
Types of delay-based timing control:
    1. Regular delay control

2. Intra-assignment delay control
3. Zero delay control Types
of event-based timing control:
1. Regular event control
2. Named event control
3. Event OR control
4. Level-sensitive timing control

15. Give the different arithmetic operators?

Operator symbol Operation performed Number of operands
* Multiply Two
/ Divide Two +
Add Two

- Subtract Two
% Modulus Two
** Power (exponent) Two

16.. Give the different bitwise operators.

Operator symbol Operation performed Number of operands

~ Bitwise negation One
& Bitwise and Two
| Bitwise or Two ^
Bitwise xor Two
^~ or ~^ Bitwise xnor Two
~& Bitwise nand Two
~| Bitwise nor Two

17. What are gate primitives?

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provide the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf(non-inverting drive buffer).

18. Give the two blocks in behavioral modeling.

1. An initial block executes once in the simulation and is used to set up initial conditions and step-by-step data flow
2. An always block executes in a loop and repeats during the simulation.

19. What are the types of conditional statements?

1. No else statement

Syntax : if ([expression]) true – statement;
2. One else statement
Syntax : if ([expression]) true – statement;
else false-statement;
3. Nested if-else-if
Syntax : if ([expression1]) true statement 1;
else if ([expression2]) true-statement 2;
else if ([expression3]) true-statement 3;

else default-statement;
The [expression] is evaluated. If it is true (1 or a non-zero value) true-statement is
executed. If it is false (zero) or ambiguous (x), the false-statement is executed.

20. Name the types of ports in Verilog

Types of port Keyword
Input port Input Output
port Output Bidirectional
port inout

21. What are the types of procedural assignments?

1. Blocking assignment
2. Non-blocking assignment

PART-B

1. Explain the concept involved in Timing control in VERILOG.

2. Explain with neat diagrams the Multiplexer and latches using transmission Gate.
3. Explain the concept of gate delay in VERILOG with example
4. Explain the concept of MOSFET as switches and also bring the various logic gates using
the switching concept.
5. Explain the concept involved in structural gate level modeling and also give the
description for half adder and Full adder.
6. What is ASIC? Explain the types of ASIC.
7. Explain the VLSI design flow with a neat diagram