Academic Year: 2017-2018

Date(s)	Type of Programme	Title	No. of Participants attended		Total	Resource Persons
			External	Internal		
03-07-2017 to 07-07-2017	Workshop	System Design and Verification using System Verilog HDL		30	30	Mr. V.Gopalakrishnan, Senior Verification Engineer, Gatwaytosilocon Technololiges Pvt Ltd., Bangalore
27-07-2017 to 28-07-2017	Workshop	Implementation of Image Processing Algorithms on FPGA		19	19	Mr.M.PeerMohamed, Research fellow, GCT, Coimbatore
23-02-2018	Workshop	Custom IC Design, CMOS Process Integration IC Fabrication, Packaging and Testing		66	66	Shri. H.S.Jatana & Ashutosh Yadav, SCL, Chandigarh, Delhi
28-09-2018 to 29-09-2018	Workshop	Implementation of Image Processing Algorithms on FPGA Hardware	4	20	24	Dr.R.Sudhakar Professor, HoD/ECE & Dr.K.N.Vijeyakumar Asso. Prof/ECE,