Academic Year: 2015-2016

Date(s)	Type of Programme	Title	No. of Participants attended		Total	Resource Persons
			External	Internal		
08.07.2015 & 09.07.2015	Workshop	Custom Digital IC Design Using CADENCE EDA Suite	10	12	22	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, AP/EEE Ms.S.Kalaiselvi, AP/ECE
28.09.2015	Workshop	Custom IC design using CADENCE EDA tool	23	9	32	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, AP/EEE Ms.S.Kalaiselvi, AP /ECE
08.10.2015	Hands on Training (EEE Association)	Custom Analog IC Design using CADENCE EDA Suite	-	33	33	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, AP/EEE
27.01.2016 & 28.01.2016	Workshop	System Design Using Xilinx Vivado Design Suite on Zynq 7000 SoC Kit	4	28	32	Mr.Prakash CoreEL Technologies, Bangalore
27.02.2016	Workshop (IEEE)	Custom Analog IC Design using CADENCE EDA Suite	-	22	22	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, APs/EEE Ms.S.Kalaiselvi,

						AP /ECE
12.03.2016	Workshop (Uddesha ’16)	Custom IC Design using CADENCE EDA Suite	27	-	27	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, APs/EEE Ms.S.Kalaiselvi
30.09.2016	Workshop (Uddesha ’16)	Custom Analog IC Design using CADENCE EDA	15	-	15	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, APs/EEE Ms.S.Kalaiselvi,AP /ECE
15.09.2016 to 16.09.2016	Workshop	Custom IC Design using CADENCE EDA	11	-	11	Dr.K.N.Vijeyakumar Asso. Prof/EEE Ms.K.Saranya & Ms.M.Sangeetha, APs/EEE Ms.S.Kalaiselvi,AP /ECE
01.10.2016 to 02.10.2016	Workshop	Recent Trends in Physical Design, Packaging,Custom IC Design using CADENCE EDA	-	52	52	SoC design Engineer, Intel Corporation Ltd, Bangalore.