Academic Year: 2016-2017

UG Projects:

Domain	S.No	Name of the Student	Guide Name	Title of the project
Analog and Mixed IC Design	1	Vigneshwaran.S Supraja.S Gayathri.V	Dr.K.N.Vijeyakumar Asso.Prof./ECE	ASIC Design Of Low power Energy Efficient Factorial Circuit
	2	Rahavi.P Aravindh Shakthi.S Subaharen.S	Dr.K.N.Vijeyakumar Asso.Prof./ECE	ASIC Implementation Of Floating Point Arithmetic Unit Using Reversible Gate
	3	Kalidha Banu.Z Karthikeyan.G Vijay Kumar.S	Ms.K.Saranya AP/EEE	Design of Radix-10 Decimal Multiplier using Reversible Logic
	4	Saranya.T Rajadurai.M Mallikarjunan.P	Ms.K.Saranya AP/EEE	Design of Comparator using Reversible Logic
	5	Hamshavani.G Arun Balaji.D Gowtham.G	Ms.S.Kalaiselvi AP/ECE	ASIC Implementation Of Energy Efficient Approximate Multiplier In FIR Filter For Signal Processing Applications
	6	Haritha.A Naveen Kumar.B Janaki.M Deepika.R	Mr.G.Anand AP/ECE	ASIC Implementation of High Speed CarryLook Ahead Adder
	6	Malar Vizhi.S Jayaprakash.K Pranesh.S Krishna Kumar.M	Ms.P.Sathyabama AP/ECE	VLSI Implementation of 2D Discrete Wavelet Transform
	7	Nandhini.E Divya.M Chinnathambi.R.M RaguhulRaj.P	Mr.P.Mohankumar AP/ECE	Energy and area Efficient CSLA using Systematic cell Design Methodology
	8	Sheela.N Gowthaman.V Harish Kumar.M	Ms.S.Kalaiselvi AP/ECE	ASIC implementation of Area Efficient Inexact Floating Point Adder
	9	Santhosh Kumar.M Vishnu.V Mahesh Kumar.S	Dr.K.N.Vijeyakumar Asso.Prof./ECE	CMOS Design of Low Noise Amplifier for RF applications
	10	Vigneshwar.M Ajeeth Kumar.S	Dr.K.N.Vijeyakumar Asso.Prof./ECE	ASIC Implementation of 16-BIT R-2R Ladder

		Karthikprasan.M		Digital to Analog Converter
	11	Muralidaran.S Revathy.S Jeevitha.R	Ms.R.L.Helen Catherine AP/EEE	Design of Phase Locked Loop using Cadence EDA Tool
	12	Akshaya.V.S Keerthi.S Karthikeyan.V	Ms.S.Kalaiselvi AP/ECE	ASIC Design of Phase Locked Loop
	13	Keerthana.M Gajendrakumar.S Varshinee.V.S	Ms.C.Kalamani AP/ECE	ASIC Implementation of Flash Analog to Digital Converter
	14	Saranya.T Gowthami.D Ganaga Rajesh.G	Mr.B.Pradeep Kumar AP/ECE	VLSI Implementation of High Sensitive Finger Print Sensor Using Charge Transfer circuit
	15	Gowtham.K Geetha Priya.S Saranya.S	Mr.K.Mahesh Kumar AP/ECE	ASIC Implementation of Carry Select Adder
	16	Deepak Prasad.U Indhumathi.S Sumathi.S.M	Mr.K.Mahesh Kumar AP/ECE	Optimization of 1-Bit Hybrid Full Adder Cell
	17	Dinesh Kumar.R Krishnamoorthi.K Nivetha Jass Bhavani.M	Ms.C.Suganya AP/ECE	ASIC Implementation of 4-Quadrant Analog Multiplier Design
	18	Abishek Karthick.V Anitha.S Kavin Kumar.K	Ms.C.Kalamani AP/ECE	Design and Implementation of Fault Tolerant Hybrid Full Adder
	19	Vijayalakshmi.K Blessy Vinodhini.S Babu Ganesh.S	Ms.S.Kalaiselvi AP/ECE	ASIC Implemetation of Energy Efficient Analog to Digital Converter
FPGA Implementation of Image and Signal Processing Applications	20	Hamsathvani.G Arun Balaji.D Gowtham.G	Ms.S.Kalaiselvi AP/ECE	FPGA Implementation of Adaptive Median Filter for Digital Images
	21	Mohamed Nivas.K Gowtham.R Tamilarasu.R	Ms.C.Suganya AP/ECE	FPGA Implemetation of Boolean Algebra Based Cryptographic Algorithm
	22	Zahid Ahamed.S Annal Mahizhini.R Hari Narayanan.B	Mr.B.Pradeep Kumar AP/ECE	Design of Low Power IP-SRAM Design Using CMOS Technology

PG Projects:

Domain	S.No	Name of the Student	Guide Name	Title of the project
Analog and Mixed IC Design	1	Archanaa.M	Mr.B.Kishore AP/EEE	High Performance Multiplier Based On Non-Redundant Radix-4 Signed Digit Encoding
	2	Hemaa.T.S	Dr.K.Umamaheswari AP/EEE	ASIC Implementation Of High Speed Redundant Binary Multiplier With Novel XOR Based RB-NB Conversion
	3	Jeba Mettil.I	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	ASIC Design Of High Speed Montgomery Modular Multiplication Architecture
	4	Senthilvel.K	Mrs.J.Amudha AP/EEE	ASIC Implementation Of IEEE 754 Truncated Floating Point Multiplier Unit
FPGA Implementation of Image and Signal Processing Applications	5	Vinothini.P	Mr.A.Nandhakumar AP/EEE	FPGA Implementation of Approximate Arithmetic Units for Video Encoding